

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
1875.2810001/RES/GSBAPPLICATION NO.
To Be AssignedFIRST NAMED INVENTOR
Jan MULDERFILING DATE
HerewithART UNIT
To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
JW	AA1	6,583,747 B1	06/2003	van der Goes <i>et al.</i>	341	156	
	AB1	6,628,224 B1	09/2003	Mulder <i>et al.</i>	341	156	
	AC1	6,518,898 B1	02/2003	Choksi	341	118	
	AD1	6,346,902 B1	02/2002	Venes <i>et al.</i>	341	154	
	AE1	6,489,913	12/2002	Hansen <i>et al.</i>	341	156	
	AF1	6,169,502	01/2001	Johnson <i>et al.</i>	341	120	
	AG1	6,259,745 B1	07/2001	Chan	375	285	
	AH1	5,867,116	02/1999	Nakamura <i>et al.</i>	341	159	
	AI1	5,973,632	10/1999	Tai	341	156	
	AJ1	5,554,943	09/1996	Moreland	327	665	
J	AK1	5,422,642	06/1995	Chung <i>et al.</i>	341	118	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Y s No
	AN1						Y s No
	AO1						Y s No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

JW	AR	1	Miyazaki, <i>et al.</i> , "A 16 mW 30Msample/s 10b Pipelined A/D Converter Using a Pseudo-Differential Architecture," <i>IEEE International Solid-State Circuits Conference 2002</i> , IEEE, February 5, 2002, 3 pages.				
	AS	1	Sushihara <i>et al.</i> , "A 7b 450Msample/s 50mW CMOS ADC in 0.3 mm ² ," <i>IEEE International Solid-State Circuits Conference 2002</i> , IEEE, February 5, 2002, 3 pages.				
	AT	1	Dingwall <i>et al.</i> , "An 8-MHz CMOS Subranging 8-Bit A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-20, No. 6, December 1985, pages 1138-1143.				

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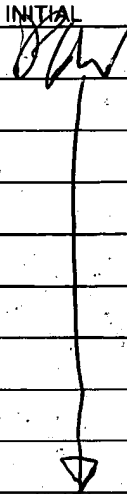
Patrick Wang

DATE CONSIDERED

05/01/2004

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Page 2 of 11							
FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">ATTY. DOCKET NO. 1875.2810001/RES/GSB</td> <td style="width: 50%;">APPLICATION NO. To Be Assigned</td> </tr> <tr> <td colspan="2">FIRST NAMED INVENTOR Jan MULDER</td> </tr> <tr> <td>FILING DATE Herewith</td> <td>ART UNIT To Be Assigned</td> </tr> </table>	ATTY. DOCKET NO. 1875.2810001/RES/GSB	APPLICATION NO. To Be Assigned	FIRST NAMED INVENTOR Jan MULDER		FILING DATE Herewith	ART UNIT To Be Assigned
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	AA2	5,471,210	11/1995	Wingender et al.	341	156	
	AB2	5,302,869	04/1994	Hosotani et al.	327	075	
	AC2	5,191,336	03/1993	Stephenson	341	111	
	AD2	5,118,971	06/1992	Schenck	326	032	
	AE2	5,157,397	10/1992	Vernon	341	159	
	AF2	5,006,727	04/1991	Ragosch et al.	327	306	
	AG2	4,959,563	09/1990	Schenck	326	627	
	AH2	3,846,712	11/1974	Kiko	330	261	
	AI2	3,697,978	10/1972	Prill	341	122	
		AJ2					
	AK2						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
	AR	2	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 34, No. 5, May 1999, pages 599-606.
	AS	2	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pages 1788-1795.
	AT	2	Bult, K. and Buchwald, A., "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm ² ," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 32, No. 12, December 1997, pages 1887-1895.

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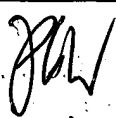


U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3						
	AB3						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Cho, T.B. and Gray, P.R., "A 10b, 20 Msample/s, 35 mW Pipeline A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 3, March 1995, pages 166-172.
	AS	3	Choe, M.-J. et al., "A 13-b 40-Msample/s CMOS Pipelined Folding ADC with Background Offset Trimming," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pages 1781-1790.
	AT	3	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35-μm CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 12, December 2001, pages 1847-1858.

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	AA4						
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	AI4						
	AJ4						
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	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

PLW	AR	4	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 33, No. 12, December 1998, pages 1932-1938.
I	AS	4	Geelen, G., "A 6b 1.1Gsample/s CMOS A/D Converter," <i>IEEE International Solid-State Circuits Conference</i> , IEEE, February 6, 2001, pages 128-129 and 438.
A	AT	4	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 μm^2 ," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pages 1796-1802.

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B. Brink Wamley

DATE CONSIDERED

8/1/04

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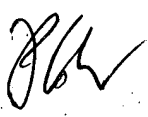
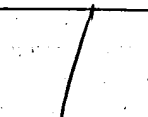
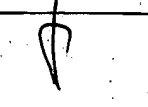
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	AA5						
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	AL5						Y s No
	AM5						Y s No
	AN5						Y s No
	AO5						Yes No
	AP5						Y s No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>5</u>	Hosotani, S. et al., "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 25, No. 1, February 1990, pages 167-172.
	AS	<u>5</u>	Ingino, J. and Wooley, B., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 33, No. 12, December 1998, pages 1920-1931.
	AT	<u>5</u>	Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 29, No. 12, December 1994, pages 1531-1536.

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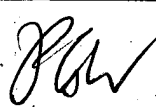


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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Y s No
	AM6						Y s No
	AN6						Y s No
	AO6						Y s No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	6	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," <i>IEEE International Solid-State Conference</i> , IEEE, 1991, pages 170-171.				
	AS	6	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 28, No. 12, December 1993, pages 1200-1206.				
	AT	6	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 27, No. 3, March 1992, pages 351-358.				

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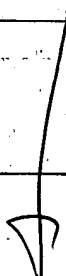

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7					
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7					Yes No
	AM7					Y s No
	AN7					Y s No
	AO7					Yes No
	AP7					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	Z	Mehr, I. And Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 3, March 2000, pages 318-325.
	AS	Z	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 8, August 1999, pages 1056-1062.
	AT	Z	Nagaraj, K. et al., "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25- μ m Digital CMOS Process," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pages 1760-1768.

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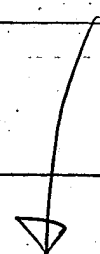

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	AA8					
	AB8					
	AC8					
	AD8					
	AE8					
	AF8					
	AG8					
	AH8					
	AI8					
	AJ8					
	AK8					

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8					Yes No
	AM8					Yes No
	AN8					Yes No
	AO8					Yes No
	AP8					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	8	Nauta, B. and Venes, A., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 12, December 1995, pages 1302-1308.
	AS	8	Pan, H. et al., "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6µm CMOS with over 80-dB SFDR," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 12, December 2000, pages 1769-1780.
	AT	8	Song, W.-C. et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 5, May 1995, pages 514-521.

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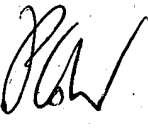

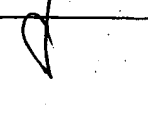
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	AA9					
	AB9					
	AC9					
	AD9					
	AE9					
	AF9					
	AG9					
	AH9					
	AI9					
	AJ9					
	AK9					

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9					Yes No
	AM9					Y s No
	AN9					Yes No
	AO9					Yes No
	AP9					Y s No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	9	Sumanen, L. et al., "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 7, July 2000, pages 1048-1055.
	AS	9	Taft, R. and Tursi, M., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 36, No. 3, March 2001, pages 331-338.
	AT	9	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b, 25-Msample/s Two-Step ADC in 0.35-μm CMOS," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 34, No. 12, December 1999, pages 1803-1811.

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	AA10					
	AB10					
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	AE10					
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	AG10					
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	AJ10					
	AK10					

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	AL10					Y s No
	AM10					Yes No
	AN10					Y s No
	AO10					Y s No
	AP10					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

PAW	AR	10	van der Ploeg, H. et al., "A 2.5-V 12-b 54-Msample/s 0.25- μ m CMOS ADC in 1-mm ² With Mixed-Signal Chopping and Calibration," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 36, No. 12, December 2001, pages 1859-1867.
	AS	10	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 32, No. 12, December 1997, pages 1876-1886.
	AT	10	Wang, Y-T. and Razavi, B., "An 8-Bit 150-MHz CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 35, No. 3, March 2000, pages 308-317.

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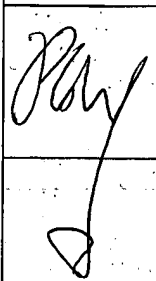

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	AA11					
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	AL11					Yes No
	AM11					Yes No
	AN11					Yes No
	AO11					Yes No
	AP11					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	11	Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 30, No. 12, December 1995, pages 1533-1537.
	AS	11	Yu, P. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," <i>IEEE Journal of Solid-State Circuits</i> , IEEE, Vol. 31, No. 12, December 1996, pages 1854-1861.
	AT	11	

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